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APPLICATION NO	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO	CONFIRMATION NO
09/683,324	12/19/2001	Kent Kuohua Chang	MXIP0085USA	6107

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NAIPO (NORTH AMERICA INTERNATIONAL PATENT OFFICE)
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EXAMINER	
MALDONADO, JULIO J	

ART UNIT	PAPER NUMBER
2623	

DATE MAILED: 03/31/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/683,324	CHANG, KENT KUOHUA
	Examiner	Art Unit
	Julio J Maldonado	2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 December 2001*

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 December 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a)☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3)☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
4)☐ Interview Summary (PTO-413) Paper No(s) _____
5)☐ Notice of Informal Patent Application (PTO-152)
6)☐ Other

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a) because they fail to show a nickel layer "38" on top of gate electrode "30" in Fig.6 and a nickel layer "64" on top of gate electrode "30" as described in the specification. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Applicants Admitted Prior Art in view of Wieczorek et al. (U.S. 6,306,698 B1), Mogami (U.S. 2001/0053601 A1) and Takayanagi et al. (U.S. 2002/0130393 A1).

In reference to claims 1 and 2, 4, 11, 12, 13 and 16, the prior art (Figs.1-6) teaches providing a semiconductor wafer (10) with a memory array area (11) and a peripheral circuit region (13) defined on a surface of a silicon substrate (12) of the semiconductor wafer (10); forming a silicon oxide layer (26) on a surface of the peripheral circuit region (13); forming a silicon layer on a surface of the silicon oxide

layer (26); patterning the silicon layer and the silicon oxide layer (26) to form a gate (30) of a MOS transistor on the surface of the substrate (12); forming a spacer (33) around the gate (30);performing a first ion implantation process for forming a lightly doped drain (LDD) of the MOS transistor; performing a second ion implantation process to form two doped areas on the substrate (12) on two sides of the gate (30); and performing a thermal annealing process to drive dopants into the two doped areas for forming the source and drain of the MOS transistor in the substrate (12) (page 1, line 23 – page 4, line 28).

The prior art fail to teach forming an amorphous silicon layer on a surface of the silicon oxide layer. However, Wieczorek et al. (Figs.2A-B) in a related method to form a MOS transistor teach forming a gate electrode layer (104) over a surface of a silicon oxide layer (105), wherein the gate electrode layer (104) material is selected from a group comprising polysilicon and amorphous silicon (column 5, lines 10 – 22). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of the prior art and Wieczorek et al. and the prior art to enable the formation of an amorphous silicon gate electrode in the prior art, and furthermore because amorphous silicon a well-known material and its selection involves common knowledge in the art.

The combined teachings of the prior art and Wieczorek et al. fail to teach forming a silicon-germanium layer on a surface of the amorphous silicon layer. Nevertheless, Mogami (Figs.4A-4E) in a related method to form a MOS transistor teaches forming a silicon germanium layer (15) over a surface of a silicon layer (14) ([0037-043).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a silicon germanium layer as taught by Mogami over a layer of amorphous silicon as taught by the prior art and Wieczorek et al., since this would reduce the depletion of the transistor ([0004]).

Still, the combined teachings of the prior art, Wieczorek et al. and Mogami fail to teach forming a nickel layer on a top surface of the gate; and performing rapid thermal annealing process for reacting the nickel layer with the silicon germanium layer on the top surface of the gate, forming a silicon nickel layer. However, Takayanagi et al. (Figs.1-7) in a related method to form a MOS structure teach forming a nickel layer on a top surface of a gate electrode (6, 7a); and performing rapid thermal annealing process for reacting the nickel layer with a silicon germanium layer (7a) on the top surface of the gate (6, 7a), forming a silicon nickel layer (15). Therefore, it would have been obvious to one of ordinary skill in the art at the invention was made to combine the teachings of Takayanagi et al. with the teachings of the prior art, Wieczorek et al. and Mogami to enable the gate of the combination to be formed, and furthermore since this would increase the conductivity of the gate transistor (0067).

In reference to claim 3, the combined teachings of the prior art, Wieczorek et al., Mogami and Takayanagi et al. teach wherein the chemical composition of the silicon germanium layer is $Si_{1-x}Ge_x$, x=0.7 (Mogami, [0038]).

In reference to claims 5, 6, 14, 15, the combined teachings of the prior art, Wieczorek et al., Mogami and Takayanagi et al. teach wherein the silicon oxide layer functions as a gate oxide layer (AAPA, page 3, line 21) of the MOS transistor, and the

amorphous silicon layer, the silicon germanium layer and the silicon nickel layer function as a gate conductive layer of the MOS transistor (Wieczorek et al., column 5, lines 10 – 22, Mogami, [0038] and Takayanagi et al., [0067]); the MOS transistor is an NMOS transistor or a PMOS transistor (Takayanagi et al., Fig.7)

In reference to claim 9, the combined teachings of the prior art, Wieczorek et al., Mogami and Takayanagi et al. teach performing a thermal annealing process diffusing germanium atoms of the silicon germanium layer into the amorphous silicon layer, transforming the amorphous silicon layer into silicon germanium (Mogami, [0040]).

In reference to claims 10 and 17, the combined teachings of the prior art, Wieczorek et al., Mogami and Takayanagi et al. teach wherein the silicon germanium layer is formed by performing chemical vapor deposition (CVD) process aerating silane and germane but fail to teach aerating hydrogen and performing the CVD process at a temperature ranging between 450°C and 620°C. However, the examiner takes official notice that hydrogen is a well-known material to use as a carrier gas in a CVD process and therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to use hydrogen because its selection involves common skill in the art. Also, these claims are prima facie obvious without showing that the claimed ranges achieve unexpected results relative to the prior art range. In re Woodruff, 16 USPQ2d 1935, 1937 (Fed. Cir. 1990). See also In re Huang, 40 USPQ2d 1685, 1688(Fed. Cir. 1996)(claimed ranges of a result effective variable, which do not overlap the prior art ranges, are unpatentable unless they produce a new and unexpected result which is different in kind and not merely in degree from the results of the prior art). See

also In re Boesch, 205 USPQ 215 (CCPA) (discovery of optimum value of result effective variable in known process is ordinarily within skill of art) and In re Aller, 105 USPQ 233 (CCPA 1955) (selection of optimum ranges within prior art general conditions is obvious).

Conclusion

4. Papers related to this application may be submitted directly to Art Unit 2823 by facsimile transmission. Papers should be faxed to Art Unit 2823 via the Art Unit 2823 Fax Center located in Crystal Plaza 4, room 3C23. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2823 Fax Center number is **(703) 305-3432**. The Art Unit 2823 Fax Center is to be used only for papers related to Art Unit 2823 applications.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Julio J. Maldonado** at **(703) 306-0098** and between the hours of 8:00 AM to 4:00 PM (Eastern Standard Time) Monday through Friday or by e-mail via julio.maldonado@uspto.gov. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri, can be reached on (703) 306-2794.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Group 2800 Receptionist** at **(703) 308-0956**.

JMR
3/13/03

George Fourson
Primary Examiner
2823